Uniport Journal of Engineering and Scientific Research (UJESR)

Vol. 8, Issue 2, 2024, Page 137-142
ISSN: 2616-1192

(www.ujesr.org)

Investigation of the Effective Negative Capacitance of Two-Port Negative Reactance Circuit from 4.48 to 4.58 GHZ and 5.7 to 5.8 GHZ

Akwuruoha, C.N

Department of Electrical and Electronic Engineering, Michael Okpara University of Agriculture Umudike, Nigeria.
*Corresponding author's email: akwuruoha.charles@mouau.edu.ng

Abstract

This paper presents an investigation of the effective negative capacitance of two-port negative reactance circuit from 4.48 to 4.58 GHz and 5.7 to 5.8 GHz. The negative reactance circuit was designed and simulated with Keysight Advanced Design System (ADS) Software and measured with vector network analyzer (VNA) at frequency range of 4.48 to 4.58 GHz and 5.7 to 5.8 GHz. The circuit was designed based on Cree CGHV4003F gallium nitride high electron mobility transistors (GaN HEMTs) biased with drain supply voltage of 20 V at quiescent drain-to-source current (I_{DSq}) of 19 mA. The two-port negative reactance circuit was fabricated on a printed circuit board using Fr_4 Microstrip substrate with dielectric constant of 4.6 and copper conductor thickness of 1.5 mm. At frequency range of 4.48 to 4.58 GHz, the measured effective negative capacitance ranged from -0.21 to -0.61 pF whereas the simulated effective negative capacitance ranged from -1.11 to -1.18 pF. At frequency range of 5.7 to 5.8 GHz, the measured effective capacitance ranged from -1.02 to -6.15 pF whereas the simulated effective capacitance ranged from -1.45 to -1.61 pF. This result indicates that the effective negative capacitance of two-port negative reactance circuit can be achieved at the selected S-band frequency ranges.

Keywords: *Two-port, Negative reactance circuit, Effective negative capacitance, GaN HEMT, Drain supply voltage, Frequency*

Received: 18th June, 2024 *Accepted: 17th September, 2024*

1. Introduction

Two-port negative reactance circuits find application in microwave devices where there is desirability to take advantage of the negative reactance characteristics of the negative impedance converters (NIC) or negative impedance inverters (NII) by delivering negative capacitance at the input impedance port while maintaining a separate output impedance port. The negative capacitance cancels out the transistor parasitic capacitance thereby enhancing the performance of the microwave circuits. The use of negative capacitance or negative inductance to enhance the performance microwave circuits has been in practice for some time. The negative impedance converters and negative impedance inverters are referred to as non-Foster circuits (NFCs). Non-Foster circuits disobey Foster reactance theorem as its reflection coefficient moves in counter-clockwise direction with respect to frequency on a Smith by chart (Kamat *et al*, 2023; Akwuruoha, 2018; Muller and Lucyszyn, 2015; Sterns, 2013; Larky, 1957; Linvill, 1953; Fano, 1948; Foster, 1924). In this paper, the effective negative capacitance of simulated and fabricated two-port negative reactance circuit at selected S-band frequency ranges of 4.48 GHz to 4.58 GHz and 5.7GHz to 5.8 GHz is investigated and reported. Negative reactance circuits referred to as non-Foster circuits find wide applications in many radio frequency (RF) and microwave circuits such as Antennas (Elfrgani and Rojas, 2015; Sussman-Fort and Rudish, 2009; Nagarkoti *et al*, 2014; Haskou et al, 2017; Hansen, 2003; Jacob et al, 2014; Koulouridis and Volakis, 2009). In addition, non-Foster circuits have reportedly been used in meta-materials (Barbuto *et al*, 2013), (Mirzaei and Eleftheriades, 2011) and power amplifiers (Lee et al, 2015; Ghadiri and Moez, 2010; Ledezma, 2015; Akwuruoha *et al*, 2017; Akwuruoha and Hu, 2017). This is the first reported investigation of the effective capacitance of GaN HEMT two-port negative reactance circuit at frequency ranges of 4.48 GHz to 4.58 GHz and 5.7 GHz to 5.8 GHz.

2. Materials and methods

The materials used in this work include Keysight's Advanced Design System (ADS) software, Cree's process design kit, Microstrip Fr_4 substrate, copper conductor, packaged Cree's CGHV4003F GaN HEMT, printed circuit board (PCB) and vector network analyzer (VNA).

2.1 Analysis of two-port negative reactance circuit

The starting point for the analysis of negative reactance circuit is the consideration of non-Foster circuit. Non-Foster circuits (NFC) can be described as open circuit stable (OCS) or short circuit stable (SCS) (Larky, 1957). The equivalent circuit of open circuit stable and short circuit stable NFCs are respectively shown in Fig. 1a and 1b.

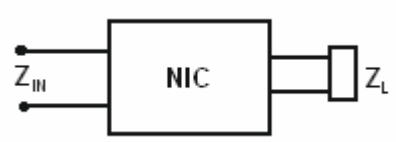

Fig. 1a: NFC equivalent circuit for open circuit stable (OCS)

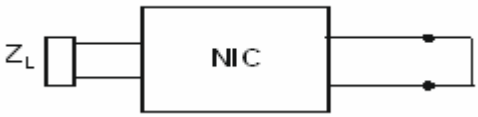

Fig. 1b: NFC equivalent circuit for short circuit stable (SCS)

In non-Foster negative reactance circuit, the driving- point impedance is equal to the negative of the load impedance and is given by (Akwuruoha, 2018).

$$Z_{in} = -KZ_L \quad (1)$$

where Z_{in} is the input impedance, K is the impedance converter coefficient and Z_L is the load impedance. The derivative of the reactance and the susceptance of the non-Foster circuit with respect to angular frequency are negative (Muller and Lucyszyn, 2015).

$$dX/d\omega < 0 \quad (2)$$

$$dB/d\omega < 0 \quad (3)$$

where X is reactance, B is susceptance and ω is angular frequency.

The driving-point impedance of a non-Foster negative reactance circuit depends on the load impedance terminating the circuit as well as circuit properties which are defined in accordance with a hybrid parameter network whereby the input/output currents (I_1/I_2) are related to the input/output voltages (V_1/V_2) by:

$$V_1/I_1 = V_2/I_2 \quad (4)$$

The equivalent circuits of a linear two-port network are shown in Figures 2a and 2b while the h-parameter equivalent circuit is shown in Fig. 2c

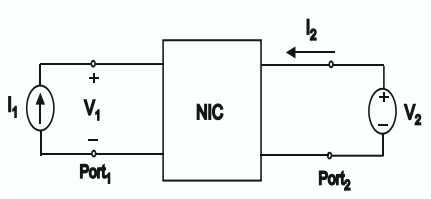

Fig. 2a: NIC as a linear two-port network

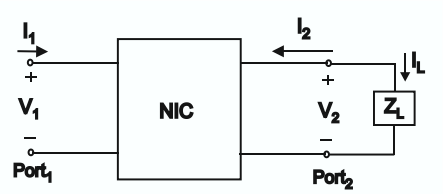

Fig. 2b: NIC as a linear two-port network with arbitrary passive load Z_L

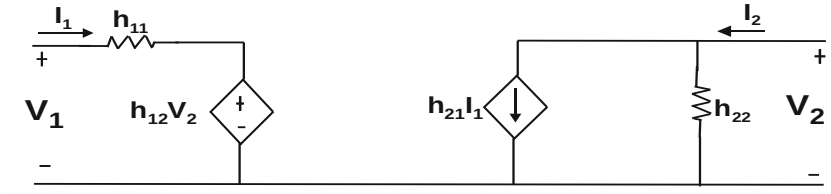

Fig. 2c: Two-port h-parameter equivalent circuit

The h-parameter equations are given by:

$$V_1 = h_{11}I_1 + h_{21}V_2 \quad (5)$$

$$V_2 = h_{21}I_1 + h_{22}V_2 \quad (6)$$

When the input port is on open circuit ($I_1 = 0$) and the output port is on short circuit ($V_2=0$), the h-parameters: h_{11}, h_{12}, h_{21} and h_{22} are respectively given by

$$h_{11} = V_1/I_1 \quad (V_2 = 0) \tag{7}$$

$$h_{12} = V_1/V_2 \quad (I_1 = 0) \tag{8}$$

$$h_{21} = I_2/I_1 \quad (V_2 = 0) \tag{9}$$

$$h_{22} = I_2/V_2 \quad (I_1 = 0) \tag{10}$$

where h_{11} is the input impedance when port 2 is on short circuit and h_{22} is the output admittance when port 1 is on open circuit. The h_{12} and h_{21} are dimensionless voltage and current ratios. The h_{12} is the reverse voltage ratio when port 1 is on open circuit while h_{21} is the forward transmission current gain when port 2 is on short circuit. If an arbitrary passive load Z_L is terminated across the output port, the driving-point impedance seen looking into the input port is given by:

$$Z_{in} = h_{11} - [(h_{12}h_{21}Z_L) / (h_{22}Z_L + 1)] \tag{11}$$

For an ideal negative impedance converter,

$$Z_{in} = -Z_L \tag{12}$$

To realize (12) from (11), the necessary conditions are:

$$h_{11} = 0 \tag{13}$$

$$h_{22} = 0 \tag{14}$$

$$h_{12}h_{21}=1 \tag{15}$$

Equations (13), (14) and (15) are true regardless of if the output terminal pairs are interchanged by terminating the arbitrary passive load Z_L to port1 or port 2. The impedance converter coefficient (K) of negative impedance converter is given by:

$$K = h_{12}h_{21} > 0 \tag{16}$$

2.2 Design

The two-port negative reactance circuit was designed and simulated with Keysight Advance Design System (ADS) software based on two Cree's CGHV40030F transistors biased with drain supply voltage of 20V at quiescent drain-to-source current (I_{DSq}) of 19 mA as shown in DC I-V characteristics bias point indicating the drain-to-source current (I_{DS}), drain-to-source voltage (V_{DS}) and gate-to-source (V_{GS}) voltage in Figure 3. The designed and simulated two-port negative reactance circuit and the one fabricated on a printed circuit board using Fr_4 microstrip substrate with dielectric constant of 4.6 and copper conductor thickness of 1.5 mm were compared at 4.48 to 4.58 GHz and 5.7 to 5.8 GHz. The two-port negative reactance circuit consists mainly of microstrip lines, capacitors and inductors.The dimension of the microstrip lines are denoted by width(mm)/length(mm). The schematic circuit of the two-port negative reactance circuit and the snapshot of the fabricated circuit are respectively shown in Figures 4 and 5.

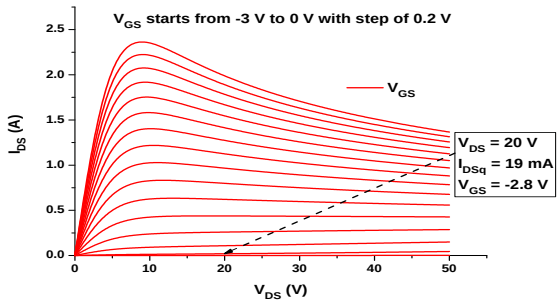

Fig. 3: DC I-V characteristics bias points

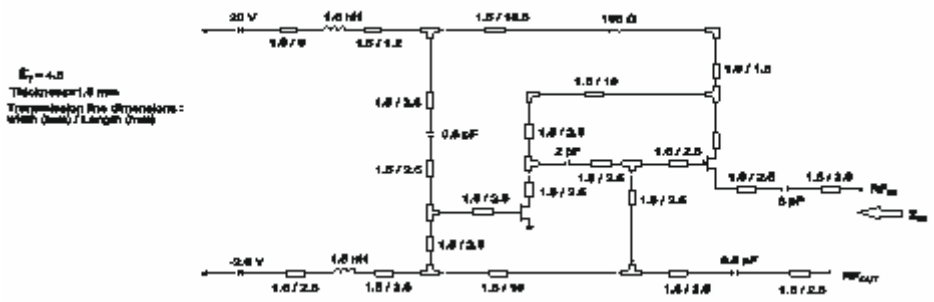

Fig. 4: Two-port non-foster circuit schematic

Fig. 5: PCB fabricated two-port negative reactance circuit

3. Results and discussion

The results of the designed and simulated two-port negative reactance circuit and the one fabricated on printed circuit board (PCB) and measured with vector network analyzer (VNA) were compared. The measurement and simulation results were obtained and compared in the first instance at 4.48 to 4.58 GHz and in the second instance, at 5.70 to 5.80 GHz. The simulation and measurement results from 4.48 to 4.58 GHz showing the magnitude and imaginary part of input impedance are shown in Fig. 6 while the effective negative capacitance is shown in Fig. 7. In Fig. 6, the two-port negative reactance circuit has negative reactance to frequency slope across the 100 MHz bandwidth. The effective negative capacitance from 4.48 to 4.58 GHz shown in Fig. 7 indicates that the two-port negative reactance circuit has measured effective capacitance ranging from -0.21 to -0.61 pF whereas the simulated effective negative capacitance from 4.48 to 4.58 GHz ranges from -1.11 to -1.18 pF. The difference in capacitance is due to the parasitic in the fabricated device.

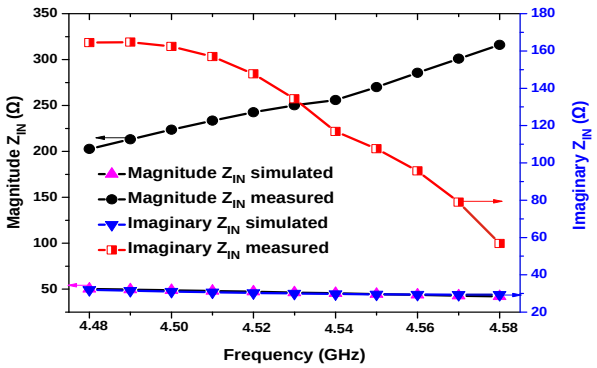

Fig. 6: Magnitude and imaginary part of input impedance from 4.48 to 4.58 GHz

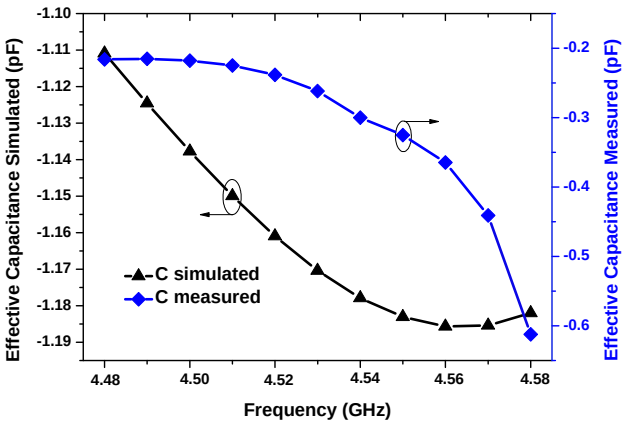

Fig. 7: Effective negative capacitance from 4.48 to 4.58 GHz

In the second instance, the two-port negative reactance circuit was measured from 5.7 to 5.8 GHz. The magnitude and imaginary part of input impedance showing negative reactance to frequency slope across the 100 MHz bandwidth from 5.7 to 5.8 GHz are shown in Fig. 8. The measured effective negative capacitance of the two-port negative reactance circuit from 5.7 to 5.8 GHz ranges from -1.02 to -6.15 pF whereas the simulated effective negative capacitance ranges from -1.45 to -1.61 pF as shown in Fig. 9. The differences capacitance is due to parasitic in the fabricated device which is more pronounced at higher frequencies.

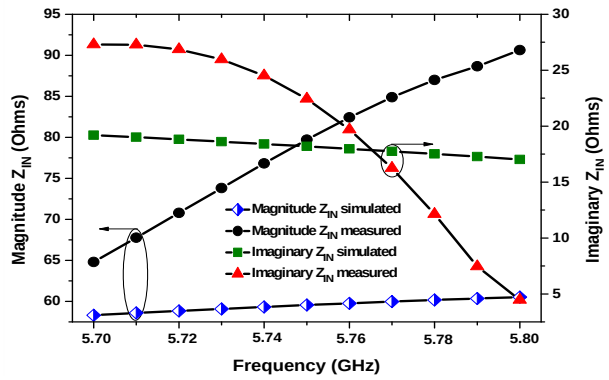

Fig. 8: Magnitude and imaginary part of input impedance from 5.7 to 5.8 GHz

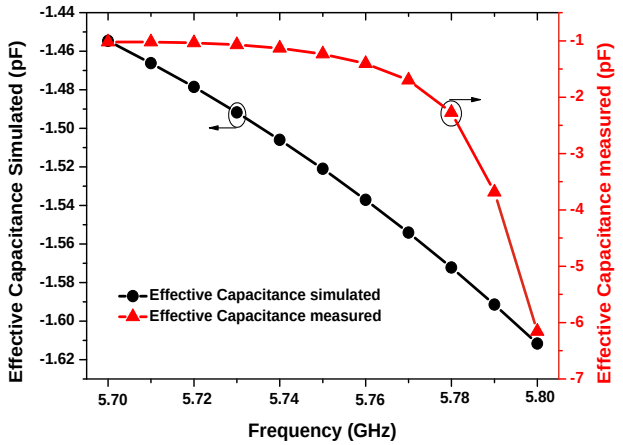

Fig. 9: Effective negative capacitance from 5.7 to 5.8 GHz

4. Conclusion

Two-port negative reactance circuit have been designed, simulated, fabricated and measured at frequencies of 4.48 to 4.58 GHz and 5.7 to 5.8 GHz. The results indicate that the fabricated and simulated negative reactance circuits consistently showed good effective negative capacitance as well as negative reactance to frequency slope across the bandwidths from 4.48 to 4.58 GHz and 5.7 to 5.8 GHz. This result indicates that the effective negative capacitance of two-port negative reactance circuit can be achieved at the selected S-band frequency ranges.

Acknowledgments

The author is grateful to Cree Incorporations USA for providing the model used in this work and The University of Manchester United Kingdom Microwave Laboratory for carrying out the measurement.

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